FPGA Implementation of High Performance Reversible Logic Method of Array Multiplier

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***Abstract*— In this recent technology of digital gadgets, digital signal processing and image processing method will have more priority, in which the arithmetic operation, such as multiplication, divisions, addition and subtractions are significant operations.. While performing these operations, arithmetic unit will have number of garbage signal with more memory logic element, due to this problem these arithmetic operation will take more area, delay and power in VLSI system design. Here, this proposed work will present a arithmetic operation using reversible logic method, thus it take memory less logic and less garbage elements, therefore here this reversible logic method is integrated using reversible half adders and full adder in array multiplier and proved the performance with less garbage signals. Finally this work is integrated in Verilog HDL, Simulated in Modelsim and Synthesized in Xilinx FPGA, and also compared all the parameter in terms of area, delay and power.**

Keywords : Reversible Logic, Array Multiplier, FPGA (Field Programmable Gate Array), LUT (Lookup Table).

I. INTRODUCTION

In Digital gadgets, applications of signal processing, image processing and video processing is most required and in that priority one is arithmetic operations with more efficiency in terms of area, delay and power. Thus, today research will focus on reduction in area, delay and power in arithmetic circuits and its operations which includes multiplication, division, addition and subtractions. For this reduction, today's technology has lot of methods. One among those methods is Reversible logic method, which is identified to as one which gives a less garbage. Reversible logic method is used in the application of quantum computing, Nanotechnology, Low power CMOS operations, Optical fiber communication, etc, This method is functions as the most priority role in reversible quantum methods. Many logic gates which are used in digital logic system like AND, OR, NAND, NOR, EXOR, EX-NOR gates are not reversible in nature. But in reversible logic system, gates are considered to have the reversible nature that is outputs can be derived from the inputs and vice versa. Reversible logic system will have the logic gates with multiple operations in, such as PERES Gate, HNG Gate, TOFFOLI Gate, FEYNMAN Gate, FREDKIN Gate, TSG Gate, SGG Gate and so on. Using such reversible logic gates the reversible structure will performed in arithmetic operations of Full adder and Full Subtractions, this addition and subtraction operations will have different structures but functionality will be same, in such as reversible gate using full adders are PERES Gate Full Adder, HNG Gate Full Adder, TOFFOLI and FEYNMAN Gate Full Adder, FREDKIN Gate Full Adder, FREDKIN and FEYNMAN Gate Full Adder, TSG Gate Full Adder, SGG Gate Full Adder. Using this Reversible logic gates it is possible to achieve reversible logic addition and subtraction and also it is possible to construct Multiplication and Division. Here, multiplication is a essential component, which is mostly used in common digital signal processing methods such as Filtering, Discrete Fourier Transform (DFT), and Discrete Wavelet Transform (DWT). Therefore to achieve a high speed processing in all digital gadgets and applications, parallel array multiplier will be widely used and its consumes more power. Here, the proposed work, parallel array multiplier designed using reversible logic gates will prove its advantages with respect to garbage signals and memory logic elements in array multipliers [1].

The operations of parallel array multiplier will have number of full adder in final addition. In this proposed work. The same is been designed with reversible logic method which proves its performance in terms of area, delay and power. In this paper, our aim to provide the consequences in less area and less power utilization using reversible logic method in parallel array multiplier with proved the effectiveness in terms of area, power and delay comparisons. Section II presents a different Full adders using reversible logic method. Section III presents a parallel array multiplier and its performance using reversible logic method. Section IV presents a FPGA Implementation of Reversible Array Multiplier architecture with results, implementation and comparisons. Section V presents a drawn conclusion of this paper with future enhancements.

II. OPERATION OF REVERSIBLE LOGIC FULL ADDER

In a arithmetic addition procedure of full adders will enclose a more critical paths, data paths with more garbage signals on digital signal processing applications and it's also take more memory elements, thus core algorithm will represents to use this full adders in address computation, division, multiplication, cache with memory access in floating

point unit (FPU) and arithmetic unit (ALU). Here, addition is one of the most basic and primary arithmetic operations which adds the two binary (1,0) digits. A circuit is said to be combinational circuit when it adds the two binary bit, it's called half adder and a circuits that sums three bits, the third bit generated from the summation of previous least significant bit (LSB), they type of circuits are known as Full Adder circuits. Full adder circuits are constructed by making use of two half adder circuits for its implementation [2]. Here, this proposed work will plan to reduced the garbage signals in conventional Full Adder circuits, so it will introduced a reversible logic Full Adders it will have multiple types such as PERES Gate Full Adder, HNG Gate Full Adder, TOFFOLI and FEYNAM Gate Full Adder, FREDKIN Gate Full Adder, FREDKIN and FEYNAM Gate Full Adder, TSG Gate Full Adder, SCG Gate Full Adder. Here, this work will implemented all the Reversible logic Full Adders and find out the efficient full adders in Reversible logic design [3]. Here, Fig.1 will shown the RTL Schematic of FREDKING and FEYNAMN Gate Full Adder, Fig.2 will shown the RTL Schematic of TOFFOLI and FEYNMAN Gate Full Adder, Fig.3 will shown the RTL Schematic of PERES Gate Full Adder, Fig.4 will shown the RTL Schematic of HNG Gate Full Adder, Fig.5 will shown the RTL Schematic of FREDKIN Gate Full Adder, Fig.6 will shown the RTL Schematic of TSG Gate Full Adder and finally Fig.7 will shown the RTL Schematic of SGG Gate Full Adder. In the Similar way the Comparison of all the reversible logic full adder will shown in Table 1, and Comparison chart will shown in Fig.8.

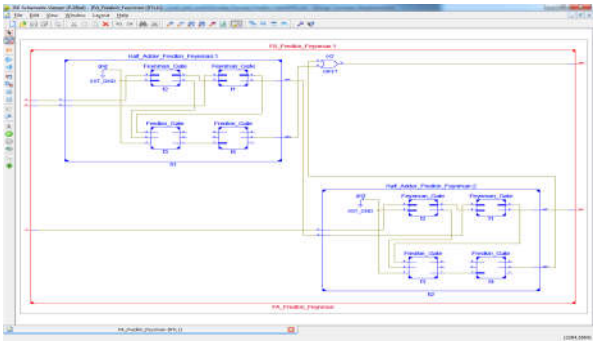

Figure 1 : Full Adder Design of FREDKIN and FEYNMAN Gate

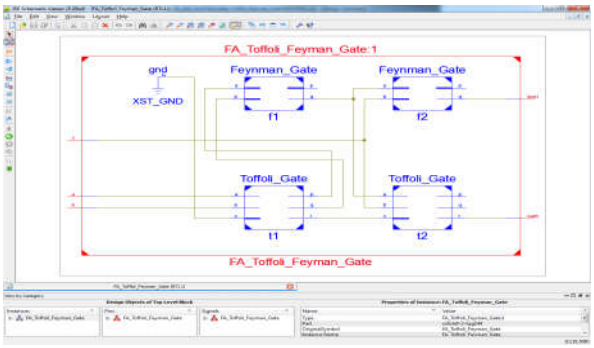

Figure 2 : Full Adder Design of TOFFOLI and FEYMAN Gate

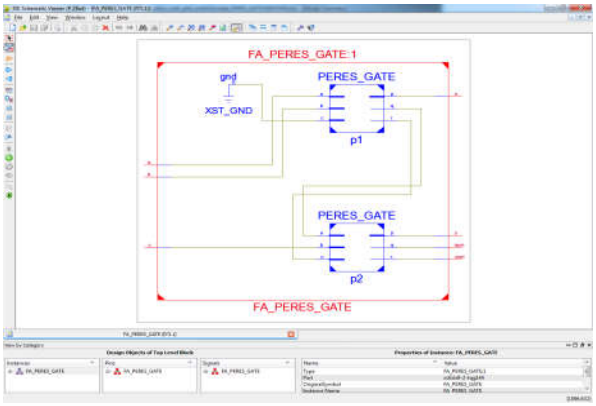

Figure 3 : Full Adder Design of PERES Gate

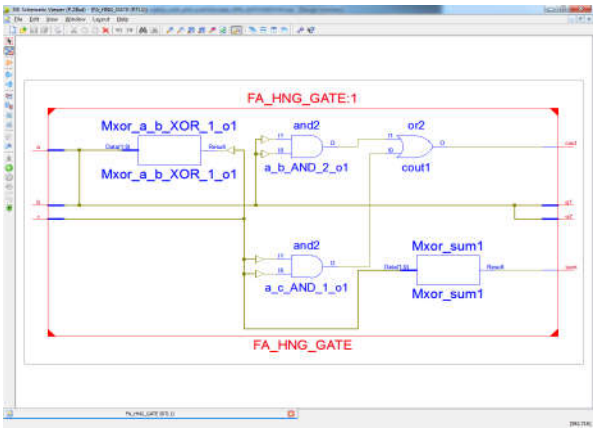

Figure 4 : Full Adder Design of HNG Gate

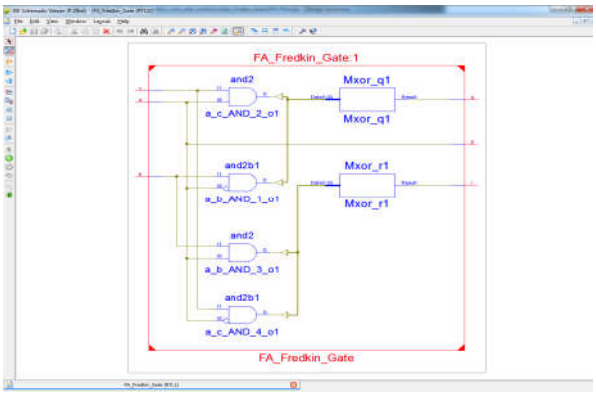

Figure 5 Full Adder Design of FREDKIN Gate

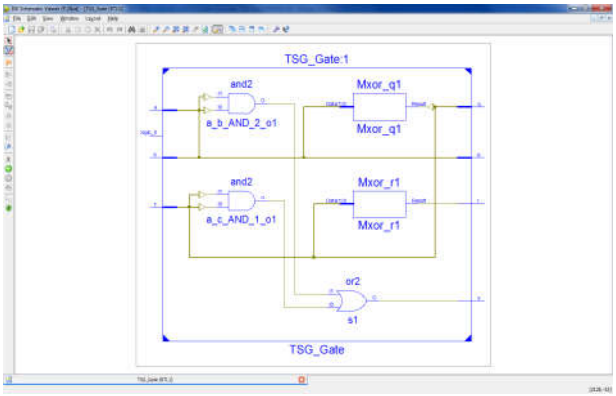

Figure 6 : Full Adder Design of TSG Gate

Table 1 : Comparison of Reversible Gate Full Adder's

Synthesized on Xilinx S6LX9 FPGA	Reversible Gate Using FULL Adder						
	PERES GATE	HNG GATE	TOFFOLI AND FEYNMAN GATE	FREDKIN GATE	FREDKIN AND FEYNMAN GATE	TSG GATE	SGG GATE
Slice Register	0	0	0	0	0	0	0
Slice LUT	2	1	1	1	1	2	1
IOB Bonded	7	7	5	6	5	7	5
Delay (ns)	6.150	6.150	6.110	6.150	6.110	6.110	6.110
Power (mW)	14	14	14	14	14	14	14

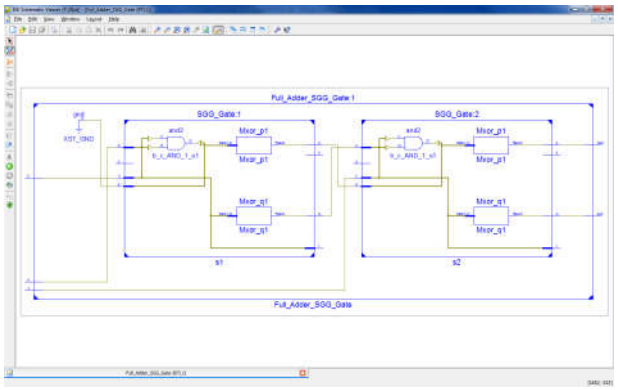

Figure 7 : Full Adder Design of SGG Gate

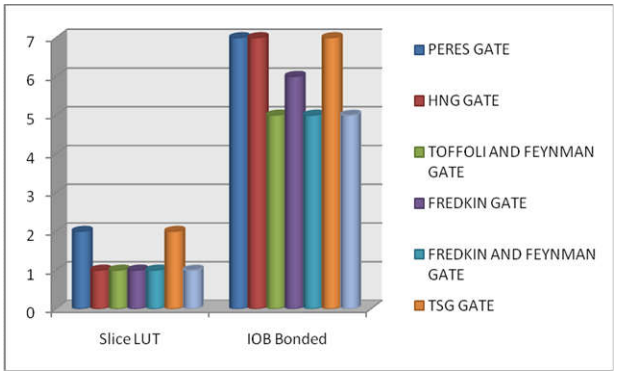

Figure 8 : Comparison LUT and IOB Chart for Reversible Full Adder Design

III. Operation of Reversible Logic Based Parallel Array Multiplier

In this method of parallel Array Multiplier will have number

of Conventional Full Adders, it will take more memory logic in Array Multiplication with garbage signals. In this proposed work of this paper will present this Parallel Array Multiplier with Reversible Logic method in this case it will reduce number of memory logic and garbage signals in Array Multiplications. Here, this paper will Compare a Parallel Array Multiplier with two reversible logic method as per the less memory logic given in Table.1 Comparisons, therefore here parallel array multiplier architecture constructed with PERES Gate and FREDKIN - FEYNMAN Gate based reversible full adder design. A initial part of this Array Multiplication is partial product generation, here this proposed work will developed at 8-Bit Array Multiplication, therefore it will take input 'A' is 8-Bit and input 'B' is 8-Bit, thus it will take 64 Partial Products example : a0b0, a0b1, a0b2, a0b3,.. .... a7b7, after this partial product generations the reversible adders will configured as per the array Multiplier architecture, it will shown in Fig.9 [4]. The Arithmetic Operation of 8x8 parallel Array Multiplier will shown in Fig.10, in this architecture included with Half adders and Full Adders, as per this proposed work will also configured reversible Half adders in this design and after this addition operation this parallel array multiplier will provide the 16-Bit Unsigned Multiplication output at S0, S1, S2, S3,.. S15 [5].

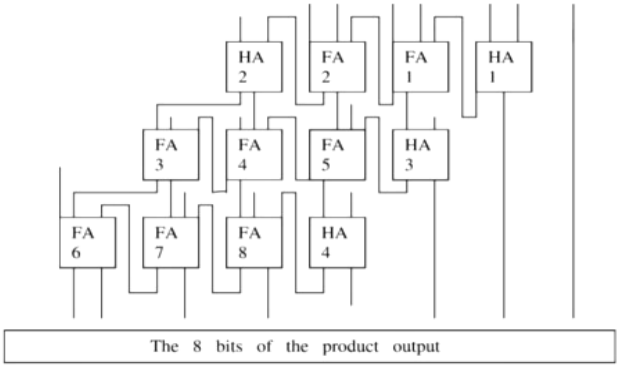

Figure 9: Parallel Array Multiplier

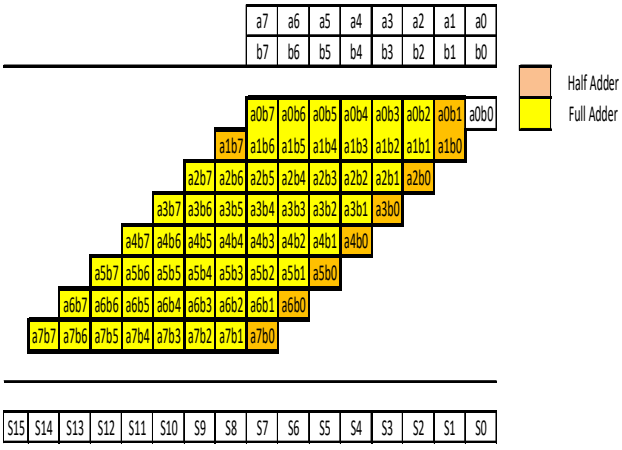

Figure 10 : Arithmetic operation of Parallel Array Multiplier

IV. FPGA IMPLEMENTATION OF PROPOSED REVERSIBLE LOGIC BASED ON PARALLEL ARRAY MULTIPLIER

Here, this proposed work of parallel array multiplier using Reversible logic method will implement in Verilog HDL, and simulated in Modelsim, and synthesized in Xilinx FPGA XC6LX9-2TQG144. Here, this PERES Gate and FEYMAN-FREDKIN Gate full adder based Reversible logic will implemented in Parallel Array Multiplier design and proved the performance of area, delay and power [6]. Here, compared this two reversible gate operation in array multiplier, will shown which one more efficient in all terms of parameters such as LUT, Slice Registers, IOB, Delay and Power. Fig.11 will shown the Simulation results of FEYMAN-FREDKIN full adder based Array Multiplier. Fig.12 will shown the Simulation results of PERES Gate based Array Multiplier. Fig.13 and Fig.15 will shown the Synthesize result from Xilinx 14.2 for FEYMAN-FREDKIN & PERES Gate full adder based Array Multiplier design, and Fig.14 and Fig.16 will shown the path delay analysis of these both parallel multiplier. Fig.17 will shown the RTL Schematic of FEYMAN-FREDKIN full adder based Array Multiplier. Fig.18 will shown the RTL Schematic of PERES Gate full adder based Array Multiplier.

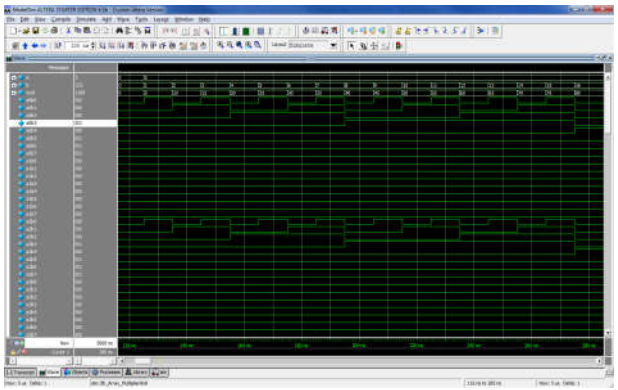

Figure 11 : Simulation output of FEYMAN - FREDKING Gate based Parallel Array Multiplier

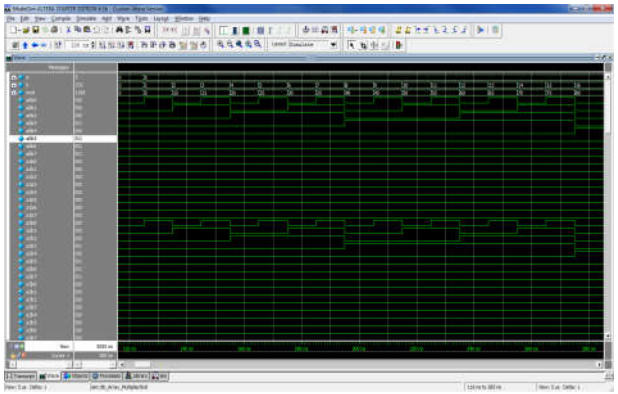

Figure 12 : Simulation output of PERES Gate based Parallel Array Multiplier

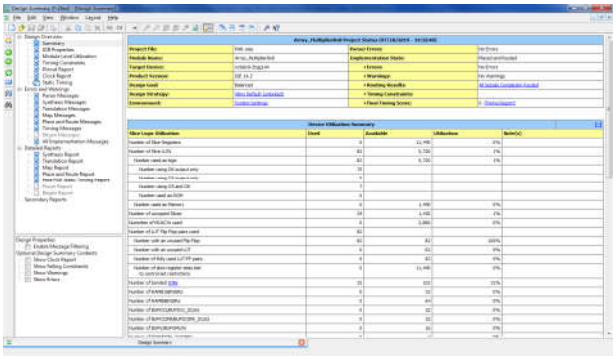

Figure 13 : Synthesize report of FEYMAN-FREDKING Gate based Array Multiplier

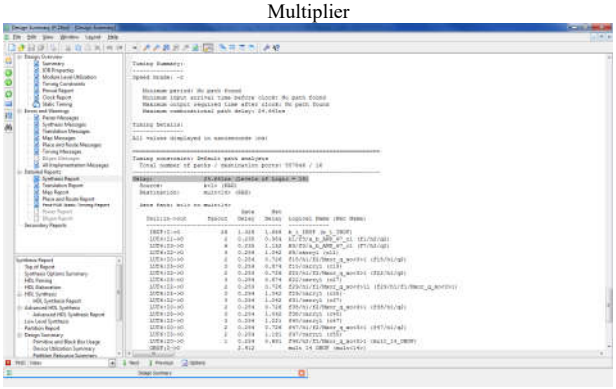

Figure 14 : Delay Report for FEYMAN-FREDKING Gate based Array Multiplier

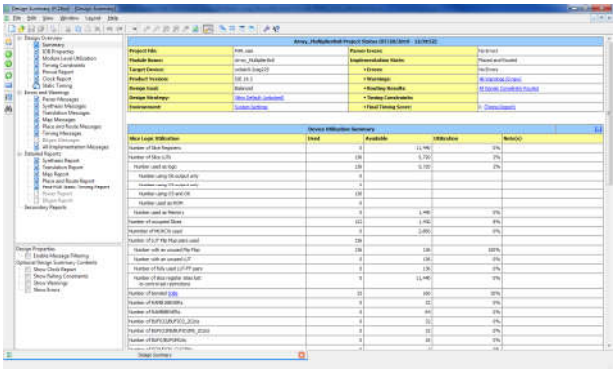

Figure 15 : Synthesize report of PERES Gate based Array Multiplier

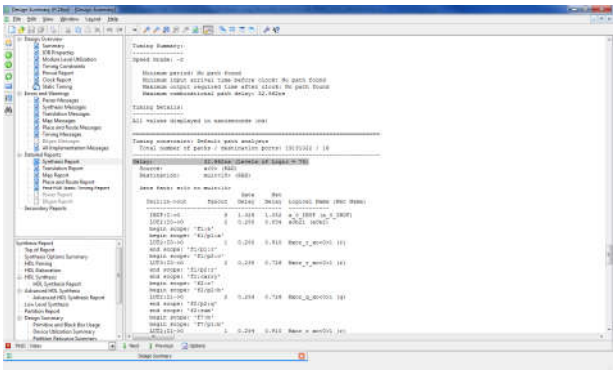

Figure 16 : Delay Report for PERES Gate based Array Multiplier

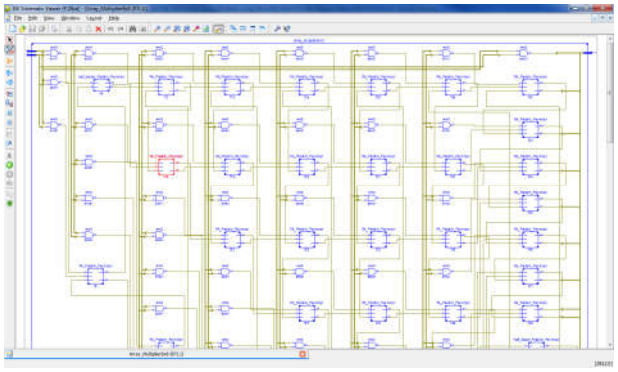

Figure 17 : RTL Schematic for FEYMAN-FREDKING Gate based Array Multiplier

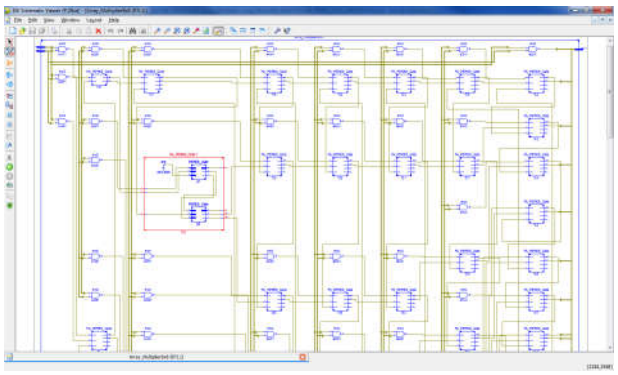

Figure 18 : RTL Schematic for PERES Gate based Array Multiplier

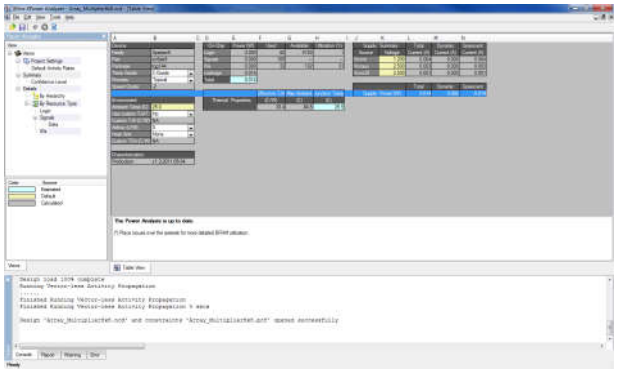

Figure 19 : Power report for FEYMAN-FREDKIN Gate based Parallel Array Multiplier

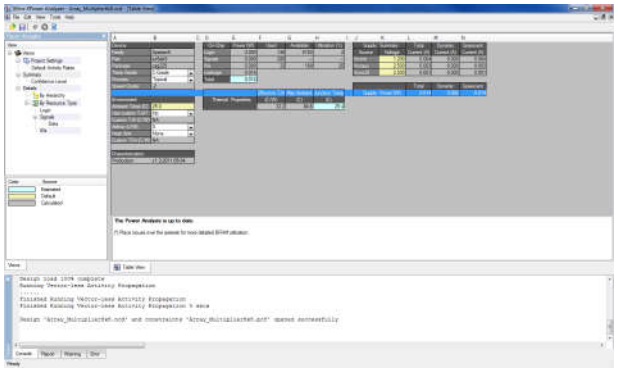

Figure 20 : Power report for FEYMAN-FREDKIN Gate based Parallel Array Multiplier

The comparison table show the LUT, IOB Bonded and Delay parameters, here Slice register will take zero in both operations because it's a combinational circuits, it not contain any Flip Flop with Clocked Operations . Power report on this comparison table and analysis will shown in Fig.19, Fig.20 it will also taken a same power, because its synthesized in Xilinx FPGA XC6LX9-2TQG144 its having 5,720 LUT but FREDKIN - FEYNMAN based array multiplier will take only 82 LUT, PERES based array multiplier will take only 136 LUT based upon this logic size power will differentiated, here power will take minimum level only, therefore its take 14 mW. Path delay will take less in FREDKIN -FEYMAN gate based Array Multiplier. Compared this PERS and FREDKIN-FEYMAN gates full design of parallel array multiplier, the FREDKIN-FEYMAN based work will take more efficient compared to PERES Gate based work it will take less LUT, and less Delay. Here, Table.2 will present this Comparisons of Parallel array multiplier using reversible logic full adder and Fig.21 will shown the analysis results of this parallel array multiplier.

Table 2 : Comparison Table for Parallel Array Multiplier using Reversible Logic Full Adder

Synthesized on Xilinx S6LX9 FPGA	FREDKIN AND FEYNMAN GATE Full Adder	PERES GATE Full Adder
Slice Register	0	0
Slice LUT	82	136
IOB Bonded	32	32
Delay (ns)	24.641	32.962
Power (mW)	14	14

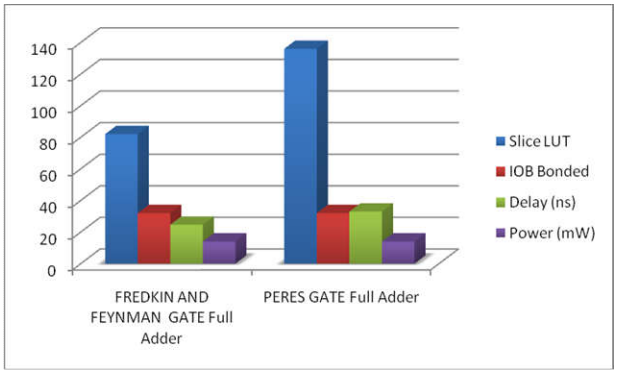

Figure 21 : Analysis of FREDKIN - FEYNMAN and PERES Gate in Parallel Array Multiplier

V. CONCLUSION

In this paper, an approach is suggested to reduced the area and power consumption in arithmetic operations, for that reasons, in this paper , the parallel array multiplier is designed in reversible logic method. This proposed work of reversible array multiplier was outperformed other parallel multiplier in terms of area, delay and power and it is proved in the comparisons. The parallel array multiplier is developed in 8-bit size and the same is simulated in Modelsim and synthesized in Xilinx S6LX9 FPGA, with compare area and power utilizations. This work is suitable to all application domain such as image processing, signal processing and gadgets based applications.

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